

2815

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PTO/SB/21 (08-00)

Approved for use through 10/31/2002. OMB 0651-0031

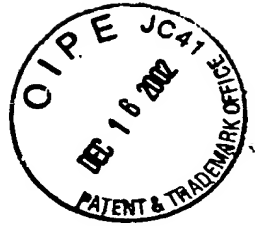
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)		Application Number	09/767,830																																	
		Filing Date	January 24, 2001																																	
		First Named Inventor	Yamada et al.																																	
		Group Art Unit	2815																																	
		Examiner Name	G. Eckert II																																	
Total Number of Pages in This Submission <<>>		Attorney Docket Number	501.39484X00																																	
<b>ENCLOSURES (check all that apply)</b>																																				
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<b>SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT</b>																																				
Firm or Individual Name	DAVID C. OREN, REG. NO. 38,694																																			
Signature																																				
Date	DECEMBER 16, 2002																																			

<b>CERTIFICATE OF MAILING</b>		
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date: December 16, 2002.		
Typed or printed name		
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TECHNOLOGY CENTER 2600

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: YAMADA et al.

Serial No.: 09/767,830

Filed: January 24, 2001

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE  
AND PROCESS FOR MANUFACTURING THE SAME

Group: 2815

Examiner: G. Eckert II

**AMENDMENT AND RESPONSE TO RESTRICTION REQUIREMENT**

Assistant Commissioner for Patents  
Washington, D.C. 20231

December 16, 2002

Sir:

In response to the Office Action dated November 14, 2002, please  
amend the above-identified application as follows:

**IN THE SPECIFICATION:**

Please replace paragraph [0112] on page 18 of the substitute  
specification with the following rewritten paragraph:

a! --[0112] With respect to the dry etching technology for forming the  
isolation trenches 2a, when an etching with large anisotropy is utilized in order to  
increase the integrity of the isolation trenches 2a, the radius of curvature of the  
bottom corner within the trenches becomes small, so that stress concentrates on the  
corner parts and transposition occurs within the semiconductor substrate 1 so as to  
degrade the element isolation characteristics.--